BK2423 Application Notes

V2.0

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Update history

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1.0	2011/01/18	BEKEN	**Initial version**
2.0	2011/05/30	BEKEN	**Update register values according to the datasheet; add different VDD values in different work status; add FAQ.**

Content

1. HOW TO JUDGE WHETHER ONE CHIP WORKS NORMALLY? 5

1.1. DIFFERENT VOLTAGE VALUES IN DIFFERENT STATUS 6
1.2. TX FAILURE ANALYSIS FLOW CHART 7
1.3. RX FAILURE ANALYSIS FLOW CHART 8

2. BK2423 MODULE RF TEST 9

2.1. TEST PREPARATION 9
2.2. TX POWER AND FREQUENCY TEST 10
2.3. TX POWER AND FREQUENCY TEST CONFIGURATION 10
2.3.1. TX Power and Frequency Test Process 10
2.4. RX SENSITIVITY TEST 11
2.4.1. RX Sensitivity Test Method 11
2.4.2. RX Sensitivity Test Process 12

3. FAQ 13

3.1. HOW TO DESIGN THE ANTENNA OF BK2423? IF I DESIGN THE ANTENNA ACCORDING TO THE HARDWARE REFERENCE DESIGN, DO I NEED ADJUST THE VALUE OF THE DEVICES? 13
3.2. HOW TO GET THE LOWEST POWER CONSUMPTION IN POWER DOWN MODE? 13
3.3. HOW TO CONTROL OUTPUT POWER? 13
3.4. HOW TO SWITCH THE CHIP TO LOW SENSITIVITY MODE, SO THAT THE DEVICES CAN COMMUNICATE WITH OTHERS AT A SHORT DISTANCE IN SOME MODES? 13
3.5. HOW TO OPERATE FEATURE REGISTERS BANK0_REG29 AND BANK0_REG7[7]=RBANK? 13
3.6. WHY SYSTEM DON'T AUTO-RETRANSMIT, WHEN ARC IS NOT 0? 14
3.7. WHAT'S THE DIFFERENCE BETWEEN EN_DPL AND EN_AA IN DIFFERENT APPLICATIONS? 14
3.8. HOW TO CLEAR MAX_RT BIT? 14

4. REFERENCE DOCUMENT 15

Chart

CHART 1 DIFFERENT VOLTAGES IN DIFFERENT STATUS---------- 6
CHART 2 TX FAILURE ANALYSIS FLOW CHART---------- 7
CHART 3 RX FAILURE ANALYSIS FLOW CHART ---------- 8
CHART 4 CONDUCTION TEST---------- 9
CHART 5 TX POWER AND FREQUENCY TEST CONNECTION----------10
CHART 6 RX SENSITIVITY TEST CONNECTION----------11
CHART 7 OUTPUT POWER CONTROL ----------13
CHART 8 DIFFERENCES BETWEEN EN_DPL AND EN_AA IN DIFFERENT APPLICATION ----------14

1. How to judge whether one chip works normally?

When one chip can't work normally, please firstly check whether the transmitter fails or the receiver fails by communicating with a good chip. And then you can debug the failure chip according to **Failure Analysis Chart.** .

(1) **Check software: whether** your code is different with the reference code, especially the reference values of registers.

(2) **Check the matching network and antenna:** whether the design of circuit and antenna are the same as the reference design, including values of parts, PCB layout and size of antenna.

(3) **No interference in ISM band:** the best way to test the interference in ISM band (2400MHz – 2483.5MHz) is to connect one 2.4G antenna to spectrum analyzer(SA), and then measure the signal in air. Set Span = 2300MHz – 2500MHz. Ref Amplitude<-50dBm. If you don't have one spectrum analyzer, you can test one channel out of ISM band. You can set one frequency out of ISM band, but BK2423 can still work. For example: set channel = 90 and the frequency is 2490MHz.

(4) **TX CW (Continuous Wave):** please refer to TX power and frequency test.

(5) **CW frequency offset <100KHz**: CW frequency offset is the difference between the measured frequency and ideal frequency. When you set channel as N, and the ideal frequency is (2400+N)MHz, please set Span<10MHz when testing.

(6) **Adjust frequency of crystal or change crystal**: please calculate the capacitors on crystal according to the load capacitance of crystal CL, C1=C2=2*CL-Cp, Cp is the parasitic capacitance on PCB, usually is 2-3 pF .If the frequency offset is still larger than 100KHz, please change the value of C1 and C2 (enlarge the value of C1 and C2 will make the work frequency lower).

(7) **Whether power supply is clean**: if the spectrum of signal carrier is very dirty, this might be caused by dirty power supply. You can use a oscilloscope to check 3.3V VDD, please set AC coupled, if the Vpp of VDD noise is larger than 20mV, which means power supply is too dirty. Please use RC filter circuit to filter the noise. Connect a serial 10 Ohm resistor and a parallel capacitor to GND. Please refer to the schematic in hardware reference design[2].
If it is very hard to make power supply clean, you can use external clean DC power to check if it can work normally.

(8) SPI read/write: write a value to a R/W register in Bank0, then read it. If the value you read is the same as the value you write, SPI read/write function is ok. If they are not the same, you can check the waveforms' time sequence and signal level..

(9) **CW locked**: whether CW is locked. Please set SA Span<1MHz, set the center frequency you expected. If the single carrier is hold on a fixed frequency and no frequency shift occurs, this means CW is locked.

(10) **Check if crystal is working normally**: crystal will be turned off in 20ms after power up, so if you want to check whether crystal works normally, you must check XTALP and XTALN pins in 20ms when power up. If there is the clock signal, the crystal is ok, or there is something wrong with the crystal.

(11) **Sensitivity test**: please refer to RX Sensitivity Test. If you have no vector signal generator, you can use PER test instead of BER test.

(12) **Check RX LO frequency offset<100KHz**: the ideal RX LO frequency is:

Frxlo=(2400+N－Fspace)*16/15MHz;

N is the channel number, Fspace＝1MHz(1Mbps,250Kbps) or 2MHz(2Mbps)。

(13) **RX LO locked**: whether RX LO is locked. Please set SA Span<1MHz, Ref Amplitude=-50dBm and the center frequency to the result of calculation according to the formula in step (12). If the single carrier is hold on a fixed frequency and no frequency shift occurs, this means RX LO is locked.

1.1. Different voltage values in different status

When one chip is in different work mode, the voltages of some pins are listed below.

	CDVDD	IREF	VDDPA	XTALP	XTALN
Default*	1.8V	0V	0V	0V	0V
Power Down	1.8V	0V	0V	0V	0V
StandByI	1.8V	0V	0V	DC is 0.7V, Vpp is 0.6V	DC is 0.7V, Vpp is 0.5V
StandByII	1.8V	0V	0V	DC is 0.7V, Vpp is 0.6V	DC is 0.7V, Vpp is 0.5V
Receive	1.8V	1.2V	0V	DC is 0.7V, Vpp is 0.6V	DC is 0.7V, Vpp is 0.5V
Transmit	1.8V	1.2	1.8V	DC is 0.7V, Vpp is 0.6V	DC is 0.7V, Vpp is 0.5V

Chart 1 Different voltages in different status

1.2. TX Failure Analysis Flow Chart

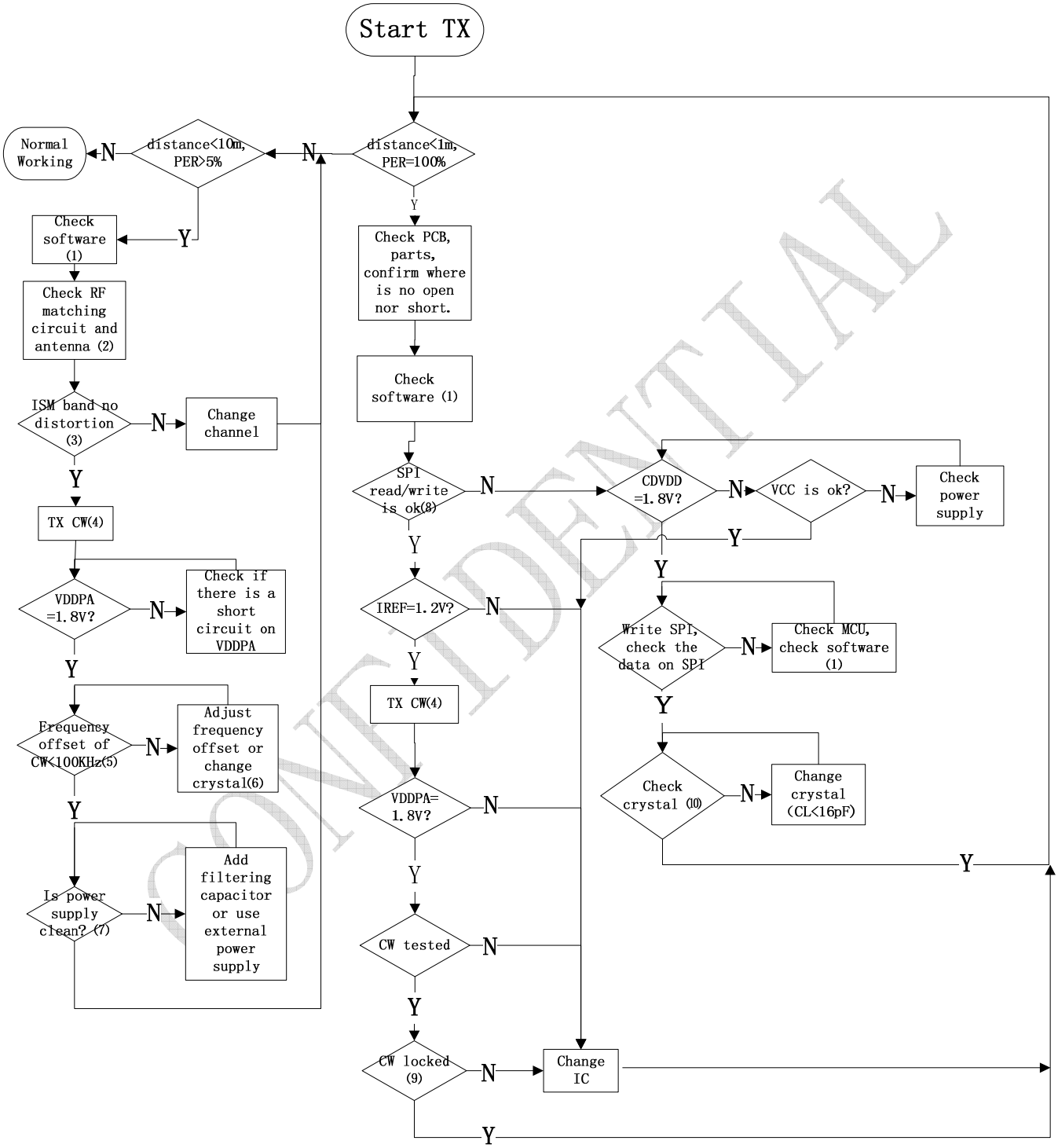

Chart 2 TX Failure Analysis Flow Chart

1.3. RX Failure Analysis Flow Chart

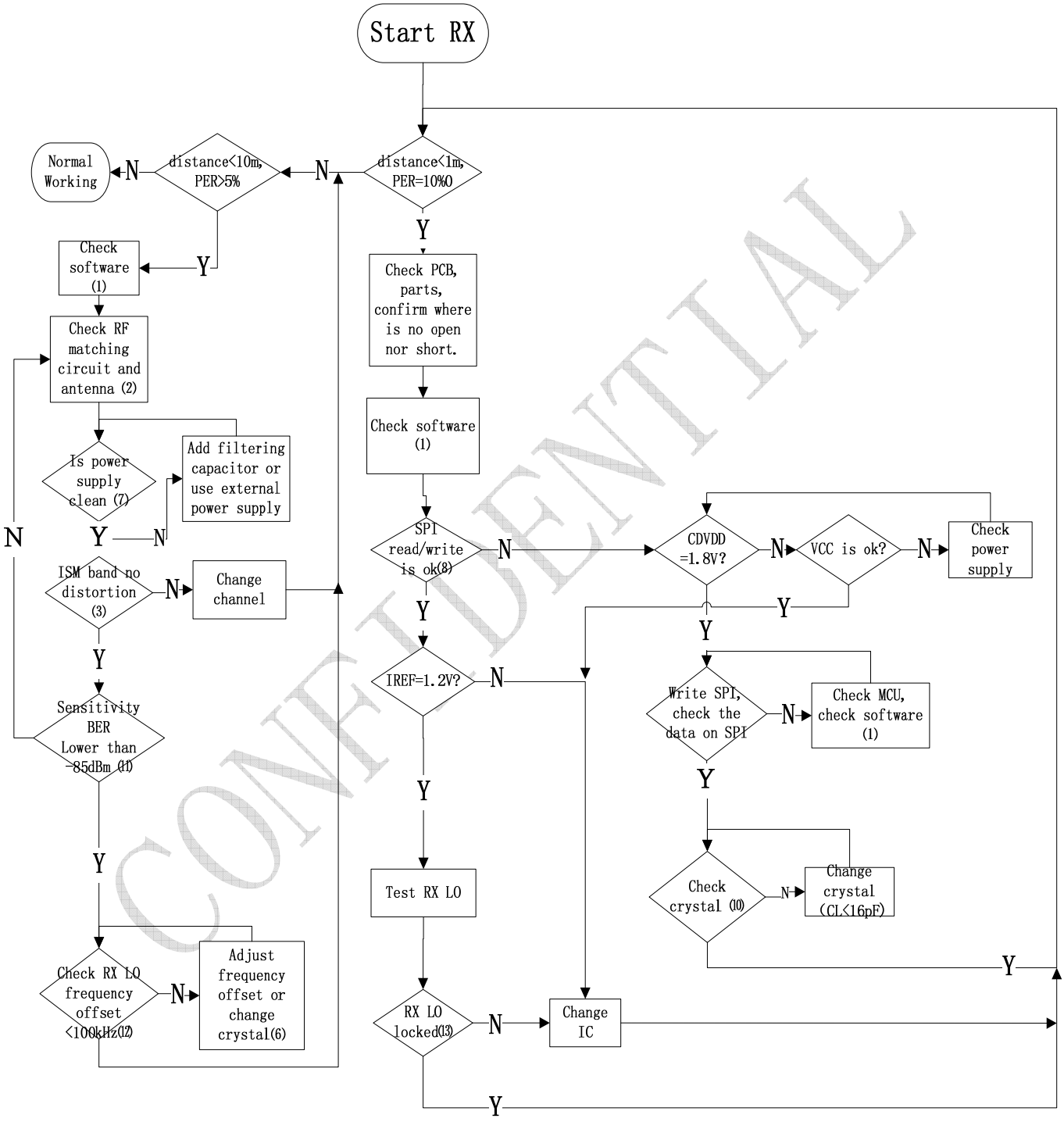

Chart 3 RX Failure Analysis Flow Chart

2. BK2423 Module RF test

The BK2423 module RF test items include transmitter output power, transmitter frequency offset and receiver sensitivity.

2.1. Test Preparation

Generally, the RF test is firstly a conduction test in the lab. A RF cable is connected between a SMA and DUT. We need to fix the cable between C5 and C6, and cut the FIPA antenna (remove L4)with the cable. The ground of RF cable should be connected to the ground of module as close as possible.

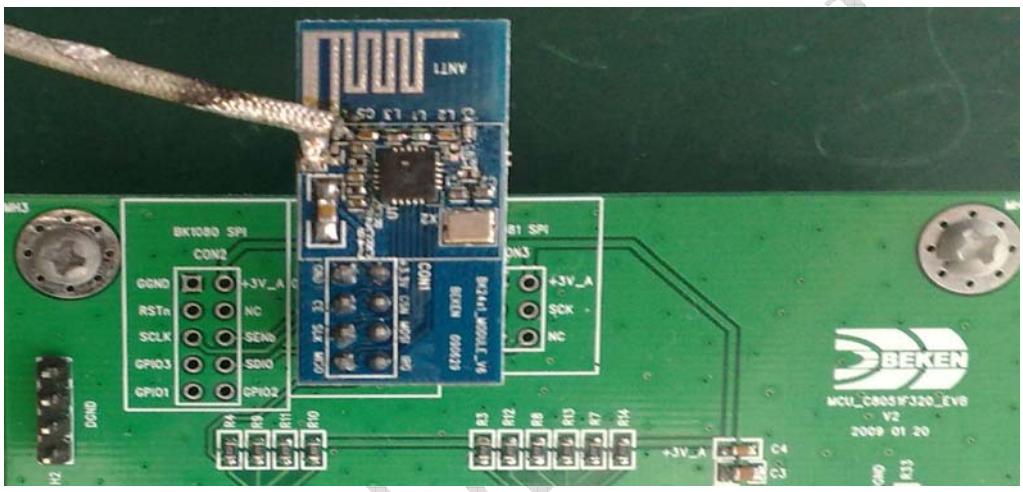

Chart 4 Conduction test

Please prepare some instruments for a RF test:

- RF test cable: we should know the insertion loss of this cable in the 2.4G band.
- Spectrum analyzer: the work frequency should be no lower than 3GHz.If you want to test the 5rd harmonics, the work frequency should be up to 13Ghz. Example models: Agilent ESA/PSA series.
- Vector signal generator: the work frequency should be no lower than 3GHz, and there is Custom (I/Q) setup modulation option. Example model: Agilent E4438C.

2.2. TX Power and Frequency Test

2.3. TX Power and Frequency Test Configuration

BK2423 DEMO board is connected to PC through USB. The spectrum analyzer is connected to demo board through RF cable.

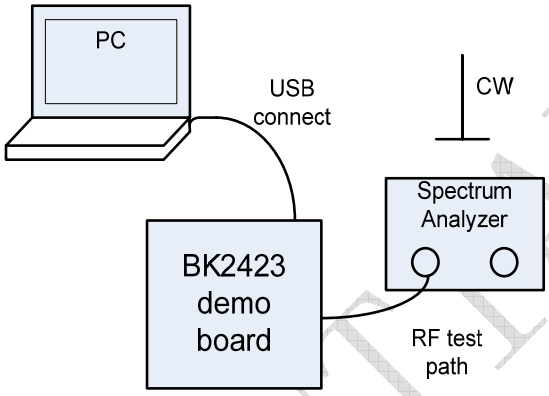

Chart 5 TX Power and Frequency Test Connection

2.3.1. TX Power and Frequency Test Process

During the TX output power and offset frequency tests, the BK2423 sends a continuous wave(CW) signal. Call the function Carrier_Test() in the reference code or use demo software directly:

(1) Switch chip to TX mode: write Bank0_REG0_Bit0=0; set CE＝1, make a rising edge on CE;

(2) Set test channel: write Bank0_REG5[6:0]=0x28=40, which is Frf＝（2400＋40）MHz;

(3) Switch to CW mode: write Bank1_REG4=0XD9BE8621; if you use Demo software, you can use “Carrier Test - Start” button at the “ACK/NoACK Mode Test” window[4];

(4) Spectrum Analyzer setting:

- Center Frequency is work frequency, such as 2440MHz at channel 40;
- Span<10MHz;
- RBW<100kHz, or Auto;

(5) Write down the frequency and output power. Go back to step (2), change channel and test again. The relationship between channel and frequency is Frf＝(2400＋channel)MHz.

2.4. RX Sensitivity Test

2.4.1. RX Sensitivity Test Method

RX sensitivity is the input signal power when RX BER (bit error rate) is 0.1%. Sensitivity can be tested in 3 ways:

(1) Calculate BER from PER:

BER can be calculated from PER (packet error rate), the formula is as below:

PER=1-(0.999^N)

N is the total bit in every packet, and the calculate result of PER is the PER value when BER is 0.1%.

In this test, ACK and Retransmit should not be used. As many as possible packets should be sent (for example 10000 packets), because the result of this method is not very accurate.

(2) Calculate BER from error bits counted by software:

Transmitter sends continuous packets to receiver. Set receiver as: No-ACK, 10 bits preamble, 3 bytes address field, No CRC.

When receiver receives the packets, it will compare them with packets already known. Then the receiver counts the number of error bits and BER. In order to get an accurate result, the total bits should be no less than 1000.

This method is a little complicate, but the result is more accurate.

(3) Calculate BER by hardware:

BK2423 has the function of counting bit stream, which can calculate the BER. The result of this method is the accurate. But it needs the signal generator to generate PN9 signal, and also needs software programming to switch the chip to BER test mode.

Next we will introduce the method of hardware counting error bits. The device connection is shown as below:

BK2423 Demo board is connected to PC through USB , and signal generator is connected to demo through RF cable.

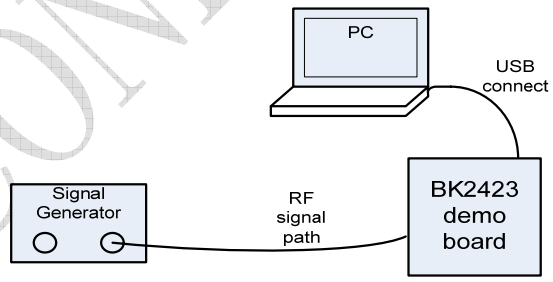

Chart 6 RX Sensitivity test Connection

2.4.2. RX Sensitivity Test Process

(1) Switch chip to RX mode: write Bank0_REG0_Bit0=1; set CE＝1, make a rising edge on CE;

(2) Set data rate to 250kbps,1Mbps or 2Mbps through Bank0_REG6_Bit3 and Bit5 registers;

(3) Work frequency calculated:

Because the frequency offset will affect the result of the test, we should measure the work frequency according to the frequency of RX LO leakage (Frxlo) before the test. Measuring Frxlo needs spectrum analyzer, please connect the devices according to TX Power and Frequency Test Connection. In RX mode, the RX LO signal will appear between 2550 and 2650MHz.

Set SA Span<1MHz, Ref Amplitude=-50dBm. Read the frequency of Frxlo. Then calculate the frequency of Frf according to the formula below:

250Kbps or 1Mbps Mode: Frf=Frxlo*15/16+1MHz
2Mbps Mode: Frf=Frxlo*15/16+2MHz

(4) Connect the module according to RX Sensitivity Test Connection. Set vector signal generator E4438C as below:

- Input Frequency: Frf(the calculate result of step (3))
- Data : PN9
- Filter : Gaussian
- Filter Bbt : 1
- Symbol Rate :250Ksps、1Msps or 2Msps
- Modulation Type : 2-Lvl FSK
- Freq Dev : 160kHz for 250ksps
  300kHz for 1Msps
  600kHz for 2Msps
- Click Button “BER Test - Start” in “ACK/NoACK Mode” window in Demo software [4]. Then click “Read” button, and adjust the output power of signal generator until the BER is 0.001. Write down the value of signal generator’s output power. This is the sensitivity of this chip. Note that the Insertion Loss of cable should be calculated.

(5) If you don’t use the demo software, you can code a function to control Bk2423. The function BER_Test() in the reference code can tell you the total bits received and total error bits received. You can calculate the BER easily.

(6) Change channel and repeat step (4), (5) and (6). You can test the sensitivity in low, middle and high frequency band.

3. FAQ

3.1. How to design the antenna of BK2423? If I design the antenna according to the hardware reference design, do I need adjust the value of the devices?

In the hardware reference design [2], we introduce some low cost PCB antenna, and the performance is accepted by most customers.

There are 2 kinds of PCB antennas in the hardware reference design: NANO PIFA antenna (used in Nano Dongle, small PCB area, but gain will be 6dB lower than normal antennas); NORMAL PIFA antenna (used in Normal Module, big PCB area, highest gain could be up to 1.5dB).

If your layout is the same as the reference layout, you needn't adjust too much. The material of the PCB is FR4, and the thickness of NANO antenna board is 0.6mm,while Normal antenna board is 1mm. If the parameters of the PCB are different, please change the antenna length or adjust L4 and C10 to match to 50Ohm using network analyzer.

3.2. How to get the lowest power consumption in power down mode?

Please set CSN high and set CE low. If there are pull-high resistors in MCU, please set CLK and MOSI high. If there are no pull-high resistors in MCU, please set CLK and MOSI low.

3.3. How to control output power?

Note that the default setting of Bank1_REG4 is 0xD9BE860B. Output power can be controlled by RF_PWR[2:0]. The highest bit RF_PWR[2] is Bank1_Reg4[20]; and the other 2 bits RF_PWR[1:0] are Bank0_Reg6[2:1]. Output power table is as below:

RF_PWR[2]= Bank1_Reg4[20]	RF_PWR[1:0]= Bank0_Reg6[2:1]	Power(dBm)
1	11	3
1	10	-2(default)
1	01	-7
1	00	-15
0	11	-25
0	10	-30
0	01	-30
0	00	-40

Chart 7 Output Power Control

3.4. How to switch the chip to low sensitivity mode, so that the devices can communicate with others at a short distance in some modes?

To communicate at a short distance, you can set Bank0_REG6[0]=0, and the sensitivity will decrease 20dB.

3.5. How to operate FEATURE registers Bank0_REG29 and Bank0_REG7[7]=RBANK?

Before read/write these registers, you should sent command ACTIVATE (+0x73 or +0x53) to activate the chip. User should read this register before activate. If the result of reading is 0, you can send

activate command. After activation you can write the value into the register. If it's activated already, it will change to un-activated mode. In un-activated mode, the return value of read operation is 0.

3.6. Why system don't auto-retransmit, when ARC is not 0?

If you want Bk2423 retransmit when error occurs, please enable Bank0_REG1=EN_AA in transmitter and receiver. For example, if you use Pipe0, please set Bank0_REG1[0]=1.

3.7. What's the difference between EN_DPL and EN_AA in different applications?

EN_DPL 和 DPL_Px	EN_AA	Description
0	0	No Enhanced Shock Burst mode.
0	1	Static payload length is defined by RX_PW_Px, the length of PTX and PRX must be same. In NOACK mode, please set REG1D[0]=EN_DYN_ACK=1, and send command W_TX_PAYLOAD_NOACK to send NOACK packet.
1	0	Dynamic payload length, send W_TX_PAYLOAD to send NOACK packet.
1	1	In NOACK mode, please set REG1D[0]=EN_DYN_ACK=1,and send command W_TX_PAYLOAD_NOACK to send NOACK packet.

Chart 8 Differences between EN_DPL and EN_AA in different application

3.8. How to clear MAX_RT bit?

When sending an ACK packet, MAX_RT interrupt will occur when retransmit times reach ARC.

MAX_RT can be clear on when there is no packet in TX FIFO. If there is packet in TX FIFO, after MAX_RT is cleared, chip will retransmit the first packet in FIFO, until send success or fail again.

So MAX_RT clear process is as below:

- Clear TX FIFO (FLUSH_TXFIFO);
- Clear MAX_RT flag(Write 1 to the register bit);

Note: RX_DR and TX_DS can be cleared by writing 1 to these 2 bits.

4. Reference Document

[1]. BK2423 Datasheet

[2]. BK2423 Hardware Reference Design

[3]. BK2423 Programming Guide

[4]. BK2423 Demo Board User Guide